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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/092,185	03/06/2002	Raymond J. Beffa	3037.10US (95-1074.10)	1655

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EXAMINER	
RODRIGUEZ, JOSEPH C	
ART UNIT	PAPER NUMBER
3653	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/092,185	BEFFA, RAYMOND J.	
	Examiner	Art Unit	
	Joseph C. Rodriguez	3653	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-3 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-3 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 06 March 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Final Rejection

Applicant's arguments filed 11/13/06 have been fully considered but they are not persuasive for reasons detailed below.

The 35 U.S.C. 112 rejections are maintained or modified as follows:

These rejections have been withdrawn.

The prior art rejections are maintained or modified as follows:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yabe (US 5,726,074) in view of Di Zenzo et al. ("Di Zenzo")(US 6,130,442).

Yabe (Fig. 5a-7b) teaches a testing method for an integrated circuit comprising storing an enhanced reliability testing flag (Fig. 7a, "Electrical Characteristics Data 3") associated with a "unique identification code" (Fig. 7a where combination of wafer ID with positional coordinates create a unique code for each chip) of each integrated circuit device of the plurality of integrated circuit devices for indicating whether each integrated circuit device requires enhanced reliability testing (col. 7, ln.

13-col. 8, ln. 10; col. 9, ln. 20-col. 10, ln. 14 teaches storing test results of specific chip that determines future quality testing of chip);

automatically reading the unique identification code of each integrated circuit device of the plurality of integrated circuit devices wherein each integrated circuit device of the plurality of integrated circuit devices forms a portion of a wafer (Fig. 6a, ID unit 3b; col. 8, ln. 1-11; col. 9, ln. 60-col. 10, ln. 4),

accessing the enhanced reliability testing flag stored for the unique identification code of each integrated circuit device of the plurality of integrated circuit devices (Id. wherein reading of "data 3" can be regarded as accessing flag);

sorting the plurality of integrated circuit devices in accordance with whether their enhanced reliability testing flag indicates they are in need of the enhanced reliability testing (Fig. 6b; col. 8, ln. 20-col. 9, ln. 18); and

performing the enhanced reliability testing for-the- each integrated circuit device of the plurality of integrated circuit devices requiring the enhanced reliability testing (Id., Fig. 6b, tester 4c).

Here, the stored information can be regarded as an "enhanced" or "further" reliability testing flag as Yabe teaches that defective chips no longer undergo testing while non-defective chips may undergo *further* sorting and testing based on narrower parameters than the original chip tester (col. 8, ln. 37-col. 9, ln. 5). That is, the use of test parameters that have been modified based on previous test results or that have been modified based on desired sorting grades can be regarded as a form of "enhanced" reliability testing as the original test parameters have been "enhanced".

Yabe as set forth above thus teaches all that is claimed except for expressly teaching said flag stored in the integrated circuit device. Di Zenzo, however, teaches the storage of enhanced testing flags on the chip (col. 2, ln.45- col. 4, ln. 30 teaching use of register to store testing information and sorting of chips based on said information so that chips can be subjected to further, i.e., enhanced, testing). Moreover, Di Zenzo expressly teaches that this type of flag storage simplifies the manufacturing process and reduces manufacturing costs (col. 5, ln. 37-48). Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the invention of Yabe as taught above.

Response to Arguments

Applicant's arguments that the prior art fails to teach the claimed features of enhanced reliability testing are unpersuasive. In particular, Yabe teaches that

> non-defective chips may undergo *further* sorting and testing based on narrower parameters than the original chip tester (col. 8, ln. 37-col. 9, ln. 5). That is, the use of test parameters that have been modified based on previous test results or that have been modified based on desired sorting grades can be regarded as a form of "enhanced" reliability testing as the original test parameters have been "enhanced".

Applicant has not adequately traversed this excerpted portion of the rejection, but has simply concluded that Yabe does not teach enhanced reliability testing. Here, Applicant is also respectfully reminded that DeZenzo was simply relied on for the teaching of storing the testing information-already taught by Yabe-within the wafer to simplify the manufacturing process and reduce manufacturing costs. Consequently, as Applicant's arguments are unpersuasive, the claims stand rejected.

Examiner has maintained the prior art rejections, statutory rejections and drawing objections as previously stated and as modified above. Applicant's amendment necessitated any new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any references not explicitly discussed above but made of record are considered relevant to the prosecution of the instant application.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Joseph C Rodriguez** whose telephone number is **571-272-6942** (M-F, 9 am – 6 pm, EST). The Supervisory Examiner is Patrick Mackey, **571-272-6916**.

The **Official** fax phone number for the organization where this application or proceeding is assigned is **571-273-8300**.

The examiner's **UNOFFICIAL Personal fax number** is **571-273-6942.**

Further, information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system.

Status information for published applications may be obtained from either Private PMR or Public PAIR. Status information for unpublished applications is available through Private PMR only.

For more information about the PAIR system, see

http://pair-direct.uspto.gov

Should you have questions on access to the Private PMR system, contact the Electronic Business Center (EBC) at **866-217-9197** (Toll Free).

Signed by Examiner Joseph Rodriguez

Jcr

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February 2, 2007